REMARKS

Claims 1-20, 22-33, and 35 are pending. Claims 6, 19, 26, and 33 have been amended.

Claims 1-20, 22-33, and 35 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Reconsideration of this rejection respectfully is requested.

The Office Action asserts that the claims contain subject matter ("shield line(s)") which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. Applicant respectfully disagrees, and notes that shield lines are shown in FIGS. 3, 4, and 5 of the application. The shield lines are described in such a way as to reasonably convey to one skilled in the relevant art that the inventor properly possessed the claimed invention.

The Office Action states that the specification discloses "shield" and "ground shield," not shield lines. Applicant notes, however, that the terms "shield" and "ground shield" in the specification refer specifically to shield lines 60 illustrated in drawing FIGS. 3, 4, and 5.

Referring more specifically to the prior art device illustrated in FIG. 3, a ground or reference shield 60 is provided "next to each signal line on the bus." See the specification at paragraph [0008], lines 3-5. Ground shields 60 are drawn in FIG. 3 as shield *lines* 60 routed alongside signal lines B0, B1, B2. Applicant notes that the shield lines 60 and the signal lines B0, B1, B2 are identically illustrated: Shield lines 60 connect between circuit element 58 and connector 52, as do signal lines B0, B1, B2. The only

exception is that, *in addition* to being routed between connector 52 and circuit element 58, shield lines 60 are coupled to ground.

Similarly, with reference to the invention illustration in FIG. 4, shield lines 60 are shown routed next to signal lines B0, B1, B2, B3. The shield lines 60 provide a coupling path from the signal lines to ground. Signal cross-talk is effectively limited to only one adjacent neighbor signal of each signal pair. See the specification at paragraph [0023], line 7 *et seq.* FIG. 5 illustrates another exemplification of the invention in which ground shields 60 are shown as lines routed along each side of a corresponding pair of signal lines B0, B1 and B2, B3.

Applicant respectfully objects to the statement in paragraph 2, page 2 of the Office Action that a shield or a ground shield "is the coupling between a pin of a connector to ground." There is no support in the application for this narrow definition of the terms "shield" or "ground shield." Instead, applicant urges that the specification and the drawings, taken properly as a whole, prevent such a narrow interpretation.

Referring again to FIGS. 3, 4, and 5, straightforward consideration reveals that shields 60 are drawn as lines that connect pins to a device as well as to ground. Thus, shields 60 are not limited to simply coupling connector pins to ground. For this and other reasons discussed further below, applicant respectfully submits that the definition applied in the Office Action to shields or ground shields is improper and unduly limits applicant's disclosure and claims.

The definition is contradicted by the teachings of the application disclosure. As an example, applicant notes that the Brief Description of the Drawings describes FIG. 3 as illustrating a circuit card having "an exemplary conventional loop-through bus topology with *shielding* provided for every signal *line*." FIG. 4 is described as

illustrating "a circuit card having a loop-through bus topology with *shielding* on every pair of signal *lines*." Similarly, FIG. 5 illustrates "a bus topology with *shielding* on every pair of signal *lines*." The drawing descriptions above become meaningless under the limited definition of "shield" or "ground shield" asserted in the Office Action. Thus, the "shield" or "ground shield" can not be merely a coupling between a pin of a connector to ground, but instead must be lines as is consistent with the disclosure and as is illustrated in the drawing FIGS. 3-5.

Applicant notes further that the prior art and inventive "shields" or "ground shields" are provided for the purpose of reducing signal cross-talk of proximate signals on the bus. Signal cross-talk is reduced by providing a ground shield "next to each signal *line* on the bus," as illustrate in FIG. 3. See paragraph 8, line 1 et seq. The Office Action's asserted definition, that the "shields" or "ground shield" are merely a coupling between a pin of a connector and ground, is contrary to the stated purpose of reducing signal cross-talk of proximate signals on the bus.

Applicant also notes that pins 62 are discussed in the specification, yet nowhere does the specification state that the "shields" or "ground shields" are there merely to couple a pin 62 to ground. Instead, as noted above, the "shields" or "ground shields" consistently are described as shielding signal *lines* from adjacent signal *lines*.

In addition, applicant notes that the Office Action's proposed use of the terms "shields" or "ground shields" is contrary to the plain meaning of the term "shield." Shield is synonymous with 'protect' or 'guard.' A mere coupling to ground for a pin does not provide a *signal line* with a *shield* as is described in the application specification and drawings.

The Office Action also considers that support is lacking for terms such as "the shield lines *removably* coupled..." Without conceding lack of support, amendments have been made to claims 6, 18, 19, and 26 to address this concern.

In view of the remarks above, claims 1-20, 22-33, and 35 comply with the written description requirement. Withdrawal of the rejection under 35 U.S.C. § 112, first paragraph respectfully is requested.

Claim 26 stands rejected under 35 U.S.C. § 112, second paragraph based on an informality due to a lack of antecedent basis. Claim 26 has been amended and particularly points out and distinctly claims the subject matter of the invention.

The Office Action contains an objection to the drawings under 37 C.F.R. § 1.83(a) on the basis that the drawings do not illustrate features recited in claim 19. Specifically, the recited features said to be missing are "a connector device having a plurality of connectors electrically connected to said processing unit and a circuit card coupled to said processing unit through said connector device."

Applicant respectfully disagrees with the basis for the objection and the application of Rule 1.83(a). The processing system 200 illustrated in FIG. 6 includes a memory circuit card 154 and a processing unit 210. See paragraph [0028] et seq. of the specification. The memory card 154 includes a connector device 152 having a plurality of connectors electrically connected to the processing unit. See FIG. 4 and accompanying text. 37 C.F.R. § 1.83(a) allows that "conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, *should* be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box)."

The drawings comply with Rule 1.83(a). Withdrawal of the objection respectfully is requested.

Claims 1-2, 5-9, 11-12, 14-16, 18-20, 24, 26-27, 29-31, and 33[1] stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,658,530 to Robertson et al. Applicant respectfully requests reconsideration of this rejection.

Claim 1 recites a circuit card that includes, *inter alia*, "a circuit element supported by the circuit card, the circuit element having a plurality of inputs and outputs," and "a plurality of signal lines supported by the circuit card, each signal line being coupled respectively to one of said plurality of inputs or one of said plurality of outputs." A "plurality of shield lines" is "supported by the circuit card." The signal lines are "grouped in a plurality of adjacent corresponding pairs, a shield line being located respectively on each side of each of said plurality of corresponding pairs of said signal lines."

Robertson et al. discloses a circuit card that features a large number of grounded pins. More specifically, Robertson et al. discloses that "the large number of ground pins may improve signal integrity by minimizing or eliminating crosstalk between signal *pins*." See Robertson et al., col. 2, lines 48-50. Robertson et al. also teaches that "the large number of electrical ground pins may help reduce interference, or "crosstalk", between signal pins." Robertson et al., col. 3, line 66- col. 4, line 1. In addition, Robertson et al. discloses that "since a large number of signal pins are located adjacent to a ground pin, signal integrity may be improved, as the ground pins may be effective in eliminating signal interference (i.e. "crosstalk"). Robertson et al., col. 5, lines 17-18.

[1] The Office Action mistakenly lists canceled claims 21 and 34 in the rejection at paragraph 4 on page 4.

In addition, applicant notes that FIGS. 1A and 1B of Robertson et al. show signal lines 103 routed between signal pins 104 and circuit element 107. Significantly, no ground shield *line* is routed between ground pin 106 and circuit element 107. Instead, FIGS. 1A and 1B show ground pin 106 coupled directly to ground and only to ground.

Robertson et al. does not teach a circuit card featuring "a plurality of signal lines supported by the circuit card, each signal line being coupled respectively to one of said plurality of inputs or one of said plurality of outputs" and "a plurality of shield lines supported by the circuit card," wherein "said signal lines are grouped in a plurality of adjacent corresponding pairs, a shield line being located respectively on each side of each of said plurality of corresponding pairs of said signal lines."

Claim 1 is not anticipated by Robertson et al. Claims 2 and 5 depend directly from claim 1 and are patentable over Robertson et al. for at least the same reasons.

Claim 6 recites a circuit card including, *inter alia*, "a plurality of shield lines supported by the circuit card, the shield lines being arranged and configured to be electrically coupled at a first end to respective connectors of said connector device mounted on said printed circuit board, each shield line being electrically coupled at a second end to a respective one of said plurality of circuit element inputs or outputs." The signal lines are "grouped in a plurality of adjacent corresponding pairs, a shield line being located respectively on each side of each of said plurality of corresponding pairs of said signal lines."

As noted above with respect to claim 1, Robertson et al. does not disclose "shield lines" supported on a circuit card "each shield line being electrically coupled at a second end to a respective one" of a plurality of "circuit element inputs or outputs."

Robertson et al. therefore also does not teach "a shield line being located respectively on each side of each of said plurality of corresponding pairs of said signal lines."

Claim 6 is not anticipated by Robertson et al. Claim 7 depends directly from claim 6 and is patentable over Robertson et al. for at least the same reasons.

Claim 8 recites a circuit card including, *inter alia*, "a plurality of signal lines having a length arranged and configured to connect between a connector device and a circuit element, supported by the circuit card, to conduct signals therebetween, said plurality of signal lines being grouped in adjacent corresponding pairs," and "a shield line extending adjacent and the length of each respective signal line pair to provide a shield, a shield line being located on each respective side of each corresponding pair of said signal lines."

As noted above, Robertson et al. teaches grounded pins. Robertson et al. does not teach "shield lines," and does not teach a circuit card featuring "a plurality of signal lines having a length arranged and configured to connect between a connector device and a circuit element, supported by the circuit card, to conduct signals therebetween, said plurality of signal lines being grouped in adjacent corresponding pairs," and "a shield line extending adjacent and the length of each respective signal line pair to provide a shield, a shield line being located on each respective side of each corresponding pair of said signal lines."

Claim 8 is patentable over Robertson et al. Claim 9 depends directly from claim 8 and is patentable over Robertson et al. for at least the same reasons.

Claim 11 recites a memory expansion card that includes, *inter alia*, "a plurality of signal lines supported by the expansion card." A "plurality of inputs and outputs" of a memory device is "coupled to a respective one of said signal lines, said signal lines being grouped in a plurality of adjacent corresponding pairs." A plurality

of shield lines is "electrically connected to said memory device, a shield line being located respectively between each pair of said plurality of corresponding pairs of said signal lines."

Robertson et al. teaches a circuit card with a large number of grounded pins. Robertson et al. does not teach a memory expansion card having a plurality of shield lines "electrically connected to [a] memory device, a shield line being located respectively between each pair of [a] plurality of corresponding pairs of said signal lines."

Claim 11 is patentable over Robertson et al. Claims 12 and 14 depend directly from claim 11 and are patentable over Robertson et al. for at least the same reasons.

Claim 15 recites a memory expansion card that includes, *inter alia*, "a memory device supported by said expansion card and having a plurality of inputs and outputs," and "a plurality of signal lines supported by said expansion card, each signal line connected respectively to one of said inputs or outputs, said plurality of signal lines being grouped respectively in adjacent corresponding pairs." A plurality of shield lines is "supported by said expansion card and electrically connected to said memory device, respective ones of said plurality of shield lines being located to extend along and between each of said plurality of corresponding pairs of said signal lines."

Robertson et al. does not disclose "shield lines." Instead, Robertson et al. discloses grounded pins. More specifically, the grounded pins disclosed by Robertson et al. are not a plurality of shield lines "supported by said expansion card and electrically connected to said memory device, respective ones of said plurality of shield lines being located to extend along and between each of said plurality of corresponding pairs of said signal lines."

Claim 15 is patentable over Robertson et al. Claim 16 depends directly from claim 15 and is patentable over Robertson et al. for at least the same reasons.

Claim 18 recites a memory expansion card assembly that includes, *inter alia*, a connector device "mounted on a motherboard and having a plurality of connectors, said plurality of connectors having a first portion for conducting signals and a second portion for providing a shield." The connectors in the first portion are "grouped in a plurality of corresponding pairs, a respective one of said connectors in said second portion being located between each of said plurality of corresponding pairs of said first portion of said plurality of connectors." A plurality of signal lines on the expansion card is "connected respectively to each of said first portion of connectors," and "a plurality of shield lines on said expansion card being connected respectively to each of said connectors in said second portion and extending respectively along adjacent signal lines connected to said first portion of connectors."

Robertson et al. discloses a memory expansion card with grounded pins, and not "shield lines on said expansion card being connected respectively to each of said connectors in said second portion and extending respectively along adjacent signal lines connected to said first portion of connectors."

Claim 18 is patentable over Robertson et al.

Claim 19 recites a processing system that includes, *inter alia*, a circuit card with "a plurality of signal lines supported by the circuit card, each of said plurality of signal lines being coupled respectively between one of [a] plurality of inputs and one of [a] plurality of connectors, or one of [a] plurality of outputs and one of [a] plurality of connectors." A plurality of shield lines is "supported by the circuit card, each shield line being coupled respectively to said circuit element, said signal lines being grouped

in a plurality of adjacent corresponding pairs, a shield line being located between respective corresponding pairs of said signal lines."

Robertson et al. teaches a processing system with a circuit card that has ground pins, not shield lines "supported by the circuit card, each shield line being coupled respectively to [a] circuit element, said signal lines being grouped in a plurality of adjacent corresponding pairs, a shield line being located between respective corresponding pairs of said signal lines."

Claim 19 is patentable over Robertson et al. Claims 20 and 24 depend directly from claim 19 and are patentable over Robertson et al. for at least the same reasons.

Claim 26 recites a processing system that includes, *inter alia*, a memory expansion card and "a plurality of signal lines and a plurality of shield lines supported by said memory expansion card." Each of a first portion of the plurality of inputs and outputs of the memory device is "coupled to a respective signal line to receive signals from or send signals to respective ones of said connectors of said connector device." The signal lines are "grouped in a plurality of corresponding pairs, a shield line being located on each respective side of each of said plurality of corresponding pairs of said signal lines."

Robertson et al. teaches a processing system with a memory expansion card having grounded pins, not "shield lines." More specifically, Robertson et al. does not disclose a processing system with a memory expansion card that has signal lines "grouped in a plurality of corresponding pairs, a shield line being located on each respective side of each of said plurality of corresponding pairs of said signal lines."

Claim 26 is patentable over Robertson et al. Claims 27 and 29 depend directly from claim 26 and are patentable over Robertson et al. for at least the same reasons.

Claim 30 recites a processing system that includes, *inter alia*, a memory expansion card having a memory device with a plurality of inputs and outputs and "a plurality of signal lines supported by said expansion card and connected respectively to said plurality of inputs and outputs, said plurality of signal lines being grouped in a plurality of adjacent corresponding pairs." A plurality of shield lines is "supported by said expansion card and electrically connected to said memory device, a respective one of said plurality of shield lines being located to extend along each of said plurality of corresponding pairs of said plurality of signal lines."

Robertson et al. teaches a processing system with a memory expansion card having a number of grounded pins. Robertson et al. does not teach a memory expansion card having a memory device with "a plurality of inputs and outputs," "a plurality of signal lines connected respectively to said plurality of inputs and outputs," in which a plurality of shield lines is "supported by said expansion card and electrically connected to said memory device, a respective one of said plurality of shield lines being located to extend along each of said plurality of corresponding pairs of said plurality of signal lines."

Claim 30 is patentable over Robertson et al. Claim 31 depends from claim 30 and is patentable over Robertson et al. for at least the same reasons.

Claim 33 recites a method for constructing a bus system device on a circuit card. The method includes "providing a circuit element on said circuit card, said circuit element having a first plurality of connectors for conducting bus signals," "grouping said first plurality of connectors into a plurality of corresponding pairs," and

"providing a second plurality of connectors on said circuit element, said second plurality of connectors being connected to a respective shield line supported on said circuit card and extending along each side of respective pairs of signal lines supported on said circuit card and connected to each of said corresponding pairs of said first plurality of connectors."

Robertson et al. discloses a method of making a circuit card having a number of grounded pins. Robertson et al. does not teach or suggest "providing a circuit element" "having a first plurality of connectors for conducting bus signals" on a circuit card, "grouping said first plurality of connectors into a plurality of corresponding pairs," and "providing a second plurality of connectors on said circuit element, said second plurality of connectors being connected to a respective shield line supported on said circuit card and extending along each side of respective pairs of signal lines supported on said circuit card and connected to each of said corresponding pairs of said first plurality of connectors."

Claim 33 is patentable over Robertson et al.

Claims 3 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Robertson et al. in view of U.S. Pat. No. 6,216,205 to Chin et al. Applicant respectfully requests reconsideration of this rejection.

Claim 3 depends from claim 1. Claim 1 is patentable over Robertson et al. as advanced above. Chin et al. does not remedy the deficiencies of Robertson et al. Chin et al. has been cited as providing a driver to drive signals between inputs and outputs of the circuit element. A combination of Chin et al. with Robertson et al. does not provide the "shield lines" missing from Robertson et al.

Claim 1 is patentable over Robertson et al. in view of Chin et al. Claim 3 depends from claim 1 and is patentable over Robertson et al. and Chin et al. for at least the same reasons.

Claim 22 depends from claim 19. Claim 19 is patentable over Robertson et al. as advanced above. Chin et al. does not remedy the deficiencies of Robertson et al. Chin et al. has been cited to provide line drivers, not "shield lines." Claim 19 is patentable over Robertson et al. in view of Chin et al. Claim 22 depends directly from claim 19 and is patentable over Robertson et al. in view of Chin et al. for at least the same reasons.

Claims 4, 10, 13, 17, 23, 28, 32, and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Robertson et al. in view of U.S. Pat. No. 6,527,587 to Ortega et al. Applicant respectfully requests reconsideration of this rejection.

Claims 4, 10, 13, 17, 23, 28, and 35 depend directly from claims 1, 8, 11, 15, 19, 26, 30, and 35, respectively. Claims 1, 8, 11, 15, 19, 26, 30, and 35 are patentable over Robertson et al. as advanced above. Ortega et al. does not remedy the deficiencies of Robertson et al.

Ortega et al. has been cited in the Office Action to provide accommodation of differential signals, which is missing from Robertson et al. Ortega et al. does not teach or suggest the "shield lines" missing from Robertson et al. Each of claims 1, 8, 11, 15, 19, 26, 30, and 35, is patentable over Robertson et al. in view of Ortega et al., along with its respective dependent claim 4, 10, 13, 17, 23, 28, and 35.

Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Robertson et al. in view of U.S. Pat. No. 6,526,462 to Elabd. Applicant respectfully requests reconsideration of this rejection.

Claim 25 depends from claim 19. Claim 19 is patentable over Robertson et al. Elabd does not remedy the deficiencies of Robertson et al. Elabd has been cited as providing a processing unit and a circuit member on the same chip. Elabd does not combine with Robertson et al. to provide the missing "shield lines." Claims 19 and its dependent claim 25 are patentable over Robertson et al. in view of Elabd.

In view of the above amendments and remarks, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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